

Control of Current Saturation and Threshold Voltage Shift in Indium Oxide Nanowire Transistors with Femtosecond Laser Annealing

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Flexible and/or transparent electronics have attracted significant interest due to their potential applications including see-through, lightweight, and conformable products.^{1–5} In particular, nanowire transistors (NWTs) may be better suited for future display products requiring transparent electronic switches because NWTs offer higher carrier mobility than those of thin-film transistors (TFTs), as well as the low-temperature processes that are compatible with optical transparency requirements.^{2–6} High-performance NWTs typically use ZnO, SnO₂, and In₂O₃ semiconducting oxide nanowires, or aligned/random networked single-walled carbon nanotubes.^{1,2,4,6,7} Many reports have suggested that NWTs have higher performance and more stable transistor characteristics compared with amorphous silicon and polysilicon TFTs, especially on field effect mobility (μ_{eff}) and subthreshold slope (SS).^{8–11} Despite these excellent properties (high performance, high sensitivity, and high efficiency), however, there are still many issues to be resolved before NWTs can find practical digital and analogue applications. One issue is to place nanowires at the desired places of the wafer/board to form designed patterns. To manufacture integrated nanowire-circuits, it would be crucial to develop the technology to control the amount and shape of the nanowire in the course of its arrangement as well as to enhance the characteristics of nanowire elements. Another issue is to achieve highly saturated transistor current and robust semiconductor characteristics, such as uniform and controllable threshold voltages (V_{th})

ABSTRACT Transistors based on various types of nonsilicon nanowires have shown great potential for a variety of applications, especially for those that require transparency and low-temperature substrates. However, critical requirements for circuit functionality, such as saturated source-drain current and matched threshold voltages of individual nanowire transistors in a way that is compatible with low temperature substrates, have not been achieved. Here we show that femtosecond laser pulses can anneal individual transistors based on In₂O₃ nanowires, improve the saturation of the source-drain current, and permanently shift the threshold voltage to the positive direction. We applied this technique and successfully shifted the switching threshold voltages of NMOS-based inverters and improved their noise margin, in both depletion and enhancement modes. Our demonstration provides a method to trim the parameters of individual nanowire transistors, and suggests potential for large-scale integration of nanowire-based circuit blocks and systems.

KEYWORDS: threshold voltage shift · In₂O₃ · nanowires · femtosecond laser · annealing · transistors

and SS. Even though many unpassivated NWTs have been demonstrated, source-drain currents are not saturated but rather increase slightly linearly in most reports.^{2,4,7–12} Little research, to our knowledge, has been conducted to reduce such linear increase even though it is perhaps the biggest obstacle for the incorporation of NWTs in such transparent circuitry on low-temperature substrates, as current saturation is the key benefit of transistors. While high-temperature annealing or doping could be used to mitigate this problem in commercial thin-film transistors, elevated temperatures can change the properties of semiconducting nanowires, and there are difficulties in adjusting the doping level uniformly. Furthermore, these methods are in most cases incompatible with flexible device panels.

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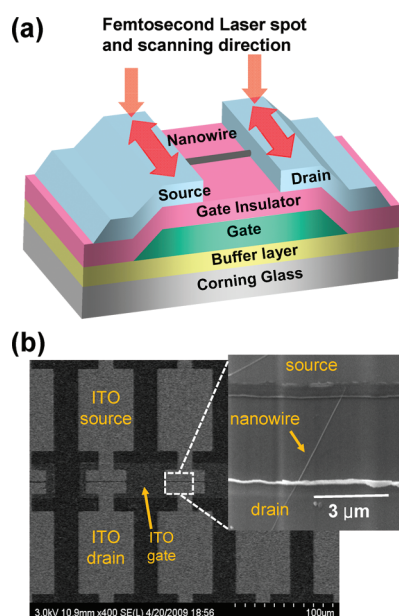


Figure 1. Schematic and scanning-electron micrograph of an In_2O_3 -based NWT. (a) The cross-sectional schematic of a fully transparent, bottom-gated nanowire transistor. The femtosecond laser pulses focus on the ITO source and drain area and scans along the edge of the source and drain pads. Laser pulses do not scan across the channel of the transistor, or the exposed portion of the nanowire. (b) Top-view scanning-electron micrograph of a fully transparent NWT. ITO was used for gate, source, and drain. The inset shows a single In_2O_3 nanowire ($D/L \approx 20 \text{ nm}/3 \mu\text{m}$) addressed between source and drain.

Here we report the effects of femtosecond laser annealing on fully transparent inverters consisting of two In_2O_3 NWTs, and show that their current saturation is improved (3–7 times increase in output resistance), and that the inverting voltages can be permanently shifted. Focused laser annealing is useful in that it can be applied selectively to small areas that require high temperatures. As a result, component damages during conventional thermal annealing of the entire panel can be avoided and unwanted effects in those areas could be excluded from the annealing process.^{13,14} In our process, we focused the laser beam spot at the contact area rather than on the nanowires themselves to avoid damaging or sputtering them away (Figure 1a). Furthermore, this annealing process could be possible even on plastic panels because instantaneous laser annealing, which is performed on a length scale of several micrometers, does not affect the temperature of the entire panel. Using this method, we demonstrated switching threshold voltage control in fully transparent NMOS inverters with the load being a diode connected n-type In_2O_3 NW transistor operated in both the enhanced mode and depletion mode.

Figure 1a is a cross-sectional view of the fully transparent NWT with the bottom gate structure, consisting of transparent glass substrate (corning glass), a buffer layer of 100 nm thick silicon dioxide, a gate electrode made from 110 nm thick patterned

indium–tin oxide (ITO), a 20 nm thick Al_2O_3 gate insulator through atomic layer deposition (ALD), a single-crystal semiconducting In_2O_3 nanowire as the active channel, and 110 nm thick ITO for source/drain (S/D) electrodes. In_2O_3 nanowires were synthesized through a laser ablation method (band gap $E_g \approx 3.6 \text{ eV}$, and diameter $D \approx 20 \text{ nm}$).¹⁵ They are transparent to visible light, and are suitable for transparent and flexible TFTs. Meanwhile, ITO is a promising candidate as transparent conductors for gate, source, and drain electrodes^{16–18} in TFTs. High- κ Al_2O_3 gate dielectric showed excellent insulating properties, with an electrical breakdown field of $>8 \text{ MV/cm}$ and a dielectric constant of ~ 9 .¹⁹ Figure 1b shows the field emission scanning electron microscope (FE-SEM) image of several NWT devices including all transparent components. The lengths of single In_2O_3 nanowire ($\sim 20 \text{ nm}$ diameter) addressed between S/D electrodes were $\sim 3 \mu\text{m}$ to avoid the complications of the short channel effects. Figure 1a also illustrates the femtosecond laser annealing process. The unique aspect of our annealing process was that laser pulses were only focused on and scanned along the S/D contact regions using its particular property of localized energy input (beam spot diameter $\sim 1.22 \mu\text{m}$). The pulse wavelengths were centered at 800 nm, which has energy below the band gap of In_2O_3 . Therefore we expected the effect to be likely different from the annealing using excimer lasers,¹³ which has a photon energy above the band gap of the nanowire.

The most prominent effects of laser annealing were the improvement of the current saturation and the positive shift of the threshold voltage V_{th} . Figure 2a shows the drain current versus drain-to-source voltage ($I_{\text{ds}}-V_{\text{ds}}$) characteristics for a representative NWT with V_{gs} ranges from -1.5 to 4 V in 0.5 V steps before (black open square) and after (red open circle) laser annealing at $0.43 \text{ J/cm}^2/\text{pulse}$. The $I_{\text{ds}}-V_{\text{ds}}$ curves of as-fabricated devices deviated significantly from the expected response of a long-channel transistor even when V_{ds} values were in the saturation region ($V_{\text{ds}} > V_{\text{gs}} - V_{\text{th}}$), and exhibited significant drain conductance or low output resistance (r_o). The annealed devices, on the other hand, appeared to have induced V_{th} shifts to the positive direction, which resulted in smaller saturation current at the same gate voltage. However, the drain currents showed significantly higher output resistance.

We first identify the threshold voltages before and after the femtosecond laser annealing. The linear-scale drain current versus gate-source voltage ($I_{\text{ds}}-V_{\text{gs}}$) of the fully transparent single In_2O_3 NWT at $V_{\text{ds}} = 0.1, 0.5$, and 4.0 V before (square) and after (circle) laser annealing is shown in Figure 2b. The V_{th} can be extrapolated from the slope of the drain current increase and the values were around -2.9 V at $V_{\text{ds}} = 0.1 \text{ V}$ and around -2.7 V at $V_{\text{ds}} = 0.5 \text{ V}$ for as-fabricated devices. However, the V_{th} values shifted along positive direction

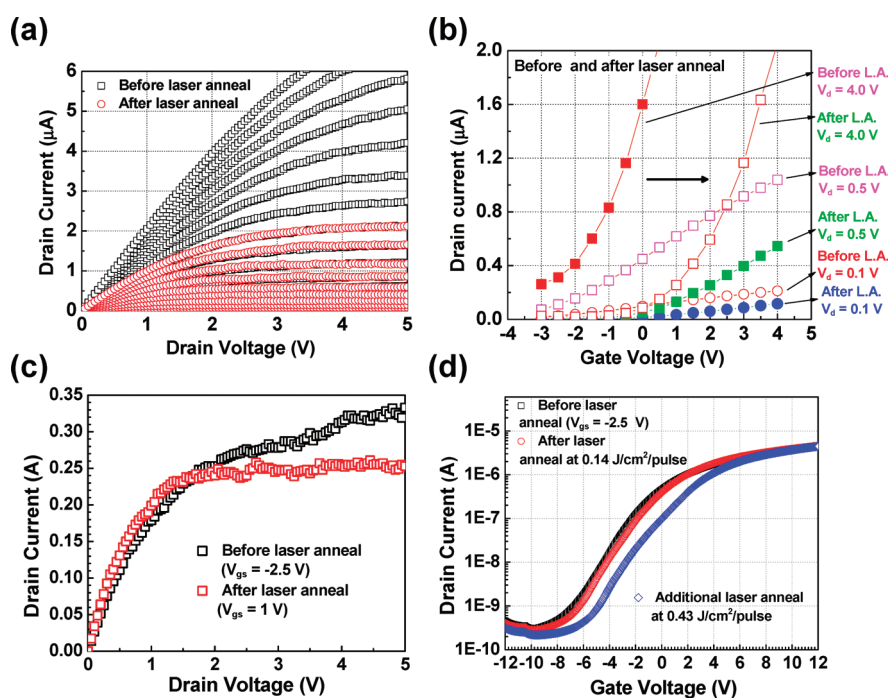


Figure 2. Effect of femtosecond laser annealing on the output resistance and threshold voltage of a NWT. (a) The $I_{ds}-V_{ds}$ characteristic of a fully transparent In_2O_3 NWT. V_{gs} ranges from -1.5 to 4 V in 0.5 V steps before (black open square) and after (red open circle) laser annealing. (b) V_{th} shift of the NWT before and after laser annealing at drain-to-source voltages of $V_{ds} = 0.1, 0.5,$ and 4.0 V. (c) The $I_{ds}-V_{ds}$ characteristic for $V_{gs} = -2.5$ V before the laser annealing (blue curve) and for $V_{gs} = 1$ V after the laser annealing (red curve). The saturation currents are similar, yet the output resistance significantly increased after laser annealing. (d) The log-scale $I_{ds}-V_{gs}$ characteristic of an In_2O_3 NWT at $V_{ds} = 0.5$ V with different power conditions: before applying femtosecond laser annealing (black open square), after $0.14 \text{ J/cm}^2/\text{pulse}$ femtosecond laser annealing (red open circle), and after an additional $0.43 \text{ J/cm}^2/\text{pulse}$ femtosecond laser annealing (blue open diamond), respectively.

to $V_{th} \approx 0.2$ and 0.5 V, respectively, after the laser annealing. Data from other V_{ds} values showed similar results and we estimate the threshold voltage to be around -2.8 V for as-fabricated NWT and around 0.4 V for annealed NWT. The apparent reduction in source-drain current after the laser annealing can thus be explained by the positive shift of the threshold voltage.

To compare the output resistance, we plotted the $I_{ds}-V_{ds}$ characteristics at $V_{gs} = -2.5$ V for the as-fabricated device, and at $V_{gs} = 1$ V for the annealed device (Figure 2c). The saturation currents were similar, as the $V_{gs} - V_{th}$ were similar (0.3 V for as-fabricated and 0.6 V for annealed NWT). For $V_{ds} > 1.5$ V, which is appreciably higher than $V_{gs} - V_{th}$, the device should be in saturation state. However, the as-fabricated device clearly showed a weak saturation, or small output resistance, while the annealed device showed strong saturation. We applied linear regression to calculate the output resistance of the transistor using $I_{ds}-V_{ds}$ data in the range of $1.5 \text{ V} < V_{ds} < 5 \text{ V}$. The output resistance for the as-fabricated transistor was $37 \text{ M}\Omega$, while for the annealed sample it was $200 \text{ M}\Omega$, showing a 5.4-fold increase. Similar increase of output resistance (3–7-fold) was observed at other saturation current values. Strong saturation is very important for almost all circuit applications requiring transistors and we believe our method is the first to achieve such a goal with extremely low thermal budget, and without

surface modification. Temporary V_{th} shifts have been reported for In_2O_3 NWTs after UV light exposure.²⁰ However, such exposure shifts the threshold to the negative direction and the device returns to its previous operation state shortly. The effect of femtosecond laser annealing appears to be permanent, and is stable in air. When we remeasured nanowire transistors after a few days and after several weeks, we observed negligible variations.

This permanent change of V_{th} suggests that the postmetallization S/D annealing with a femtosecond laser could also be a tuning method to adjust the V_{th} values of individual nanowires. To illustrate this potential, two different values of annealing power were sequentially applied to the same nanowire transistor and we observed a positive V_{th} shift after each annealing. We first measured the $I_{ds}-V_{gs}$ ($V_{ds} = 0.5$ V) of another representative NWT before laser annealing, and found the V_{th} to be -1 V, and then applied femtosecond laser annealing at $0.14 \text{ J/cm}^2/\text{pulse}$. A V_{th} shift to the positive direction by 0.5 V was observed. We then performed a second annealing on the same device, with the energy of $0.43 \text{ J/cm}^2/\text{pulse}$. A further shift toward the positive direction by 2.25 V was shown in Figure 2d. The additional power (in our case $0.43 \text{ J/cm}^2/\text{pulse}$) was essential because when we tried to apply the same annealing power, a negligible V_{th} shift was observed. Figure 2d shows the log-scale $I_{ds}-V_{gs}$ characteristics of

an In_2O_3 NWT at $V_{\text{ds}} = 0.5$ V for different annealing conditions: before applying femtosecond laser (black open square, $V_{\text{th}} = -1$ V, $I_{\text{on}}/I_{\text{off}} \approx 1.19 \times 10^4$, $SS = 2.2$ V/dec, and $\mu_{\text{eff}} = 1.12 \times 10^2$ $\text{cm}^2/\text{V}\cdot\text{s}$); after femtosecond laser annealing at pulse energy of 0.14 J/cm^2 /pulse (red open circle, $V_{\text{th}} = -0.5$ V, $I_{\text{on}}/I_{\text{off}} \approx 1.76 \times 10^4$, $SS = 2.2$ V/dec, $\mu_{\text{eff}} = 1.47 \times 10^2$ $\text{cm}^2/\text{V}\cdot\text{s}$); and after an additional femtosecond laser annealing at 0.43 J/cm^2 /pulse (blue open diamond, $V_{\text{th}} = 1.75$ V, $I_{\text{on}}/I_{\text{off}} \approx 2.23 \times 10^4$, $SS = 2.2$ V/dec, $\mu_{\text{eff}} = 1.77 \times 10^2$ $\text{cm}^2/\text{V}\cdot\text{s}$), respectively. After each femtosecond laser annealing, the $I_{\text{on}}/I_{\text{off}}$ and μ_{eff} both improved slightly. In all calculations, the field-effect mobility [$\mu = dI_{\text{ds}}/dV_{\text{gs}} \times L^2/C_i \times 1/V_{\text{ds}}$] was calculated by using the cylinder-on-plate (COP) capacitance model [$C_i = 2\pi\epsilon_0 k_{\text{eff}} L / \cosh^{-1}(1 + t_{\text{ox}}/r)$]. Therefore, femtosecond laser annealing apparently has not only improved current saturation (by increasing output resistance by 3–7-fold) but also adjusted threshold voltages of individual In_2O_3 nanowire transistors. Such effects might provide a solution to one of the long lasting problems in large scale integration of devices made from NWTs: individual trimming of NWT characteristics to match the requirements of functional devices, such as inverters, current mirrors, and amplifiers.

As an application for our capability of adjusting the V_{th} values of individual NWTs, we fabricated a fully transparent inverter with both transistors made from In_2O_3 nanowires. An inverter is one of the fundamental building blocks of logic circuits, and its switching threshold (or trip) voltage is preferred to be located at the middle of the supply voltage, which requires the proper positioning of the V_{th} values of both transistors. Moreover, high and early saturation of the transistors are also desirable to improve the noise margin by maintaining the gain in the transition region. Femtosecond laser annealing introduced here appears to be an ideal method to improve the inverter characteristics. Figure 3a shows the two types of inverters we have fabricated, one with depletion mode load (left) and the other with enhanced mode load (right). The two types of inverters are the possible candidates when there is no complementary component such as p-type nanowire MOS in the pull-up path. SEM images of depletion mode inverter with the pull-up and pull-down paths are shown in Figure 3b. Both topologies worked successfully with a supply voltage of 4 V throughout the experiments. Femtosecond laser annealing was selectively applied to individual transistors to improve the voltage transfer characteristic (VTC) of inverters, specifically the noise margins, which are defined as follows: $NM_{\text{H}} = V_{\text{DD}} - V_{\text{IH}}$, $NM_{\text{L}} = V_{\text{IL}}$, where V_{IL} and V_{IH} are input voltages at the operational points where $dV_{\text{OUT}}/dV_{\text{IN}} = -1$.

NM_{L} and NM_{H} represent noise immunity on input logic values: “0” and “1”, respectively. Thus, a balance between NM_{L} and NM_{H} is required to maximize noise immunity on both logic inputs, and the gain by the

inverter in the transition region has to be maintained high to preserve the total noise margin ($NM_{\text{L}} + NM_{\text{H}}$). As shown in Figure 3c, the laser annealing maintained transconductance (changes were insignificant) of NWT while it shifted V_{th} . This allowed us to control the switching threshold voltage of an inverter with the same gain at the switching threshold voltage (V_{M}), or trip voltage, which will maximize the noise margin of the inverter. The inset of Figure 3c shows that the hysteresis²¹ was relatively reduced after the femtosecond laser annealing. In the case of the depletion mode inverter, the diode connected NMOS (M_1) is always ON as M_1 has a negative $V_{\text{th}1}$ and its $V_{\text{gs}1}$ is fixed at 0, see Figure 3a. When the input is low (“0”) and transistor M_2 is off, M_1 keeps driving the output high until V_{ds} of M_1 drops to zero, which means that V_{OUT} is the same as the supply voltage. When the input state changes to high (“1”), M_2 starts to discharge output quickly. This can be explained by the relative magnitudes of $V_{\text{gs}} - V_{\text{th}}$ for M_2 and for M_1 , $V_{\text{gs}1} - V_{\text{th}1} = -V_{\text{th}1}$, since $V_{\text{gs}1}$ for M_1 is always 0. When $V_{\text{gs}2} - V_{\text{th}2} = V_{\text{IN}} - V_{\text{th}2}$ for M_2 is larger than $-V_{\text{th}1}$ of M_1 , the current is limited by M_1 ; and $V_{\text{ds}2}$ of M_2 quickly reduces to near zero to match the small current set by M_1 . This ensures a fast switching from high to low. Therefore the trip voltage is mostly determined by the V_{th} of M_2 and r_{o} of M_1 and M_2 , and could be smaller (1.5 V) than half of the supply voltage, 2 V, as shown in Figure 3d. To achieve enhanced noise margin, the trip voltage is preferred to be shifted to close to 2 V. NM_{H} was around 1.8 V, NM_{L} was 0.8 V, and trip voltage was 1.5 V before femtosecond laser annealing, which was smaller than half of the supply voltage and therefore reduced the low voltage input noise immunity. However, through femtosecond laser annealing, trip voltage was changed to 2.2 V, NM_{H} to around 1 V, and NM_{L} to around 1.5 V, which achieved a better balance between NM_{H} and NM_{L} . Moreover, the function of M_1 should remain complementary to that of M_2 , so the threshold voltage of M_1 had to be maintained negative while that of M_2 is shifted along the positive direction. This requires local tuning of the pull-down transistor (M_2) without significantly affecting the pull-up transistor (M_1). Our femtosecond laser annealing meets those requirements and can be applied selectively to the pull-down transistor to shift the switching voltage of inverter to be in the middle of the supply rail. The voltage transfer characteristics in Figure 3d show that enhanced noise margin was achieved by shifting the trip point of inverter from 1.5 to 2.2 V. Moreover, the hysteresis of the inverter device was modest over the bias region before and after administering the annealing. Thus, it might be possible to use this technique to control the switching threshold voltage of an inverter, which is important to achieve a high noise margin for many circuit applications.

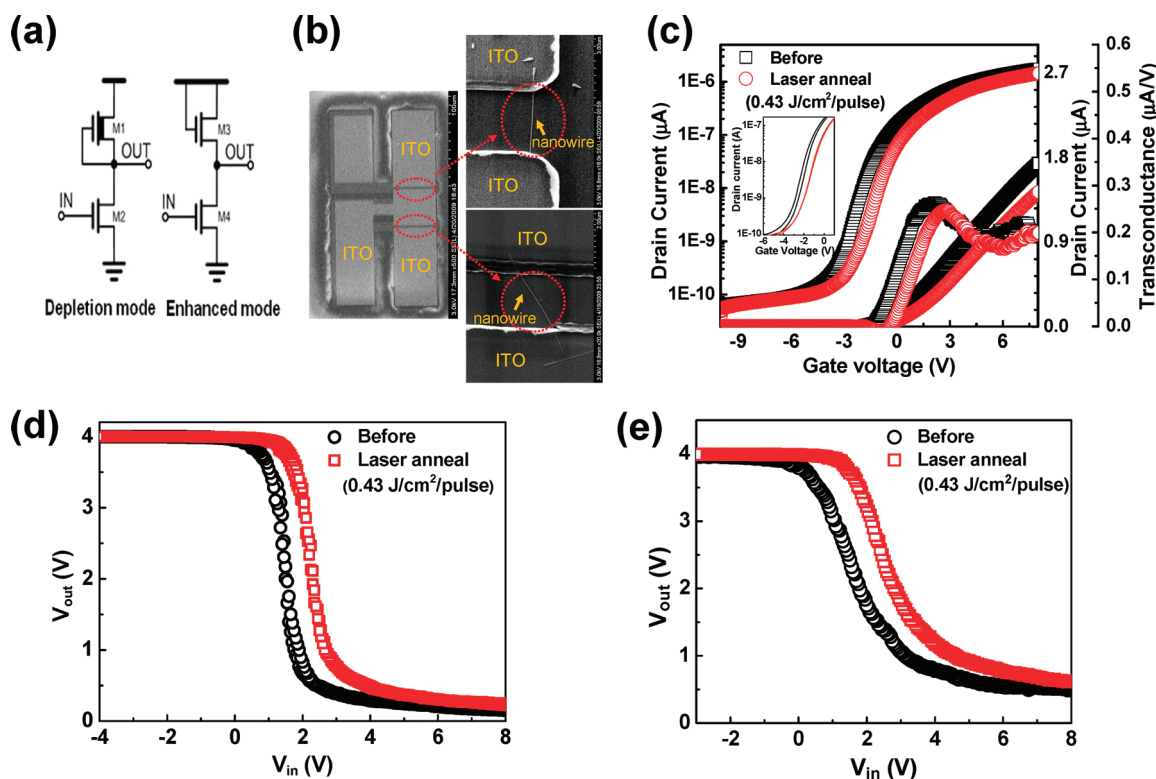


Figure 3. Shifting the switching threshold voltage of an inverter consisting of two NMOS NWTs. (a) Schematic for the circuit of depletion (left) and enhancement (right) mode inverters. (b) SEM images of depletion mode inverters with pull-up and pull-down path. (c) The drain current versus gate-source voltage ($I_{ds}-V_{gs}$) of the fully transparent single In₂O₃ NWT at $V_d = 0.5$ V. The threshold voltage (V_{th}), on-off current ratio (I_{on}/I_{off}), field effect mobilities (μ_{eff}), and subthreshold slope (SS) of NWTs before laser annealing were -0.25 V, $\sim 3 \times 10^4$, 83.6 cm² V⁻¹ s⁻¹, and ~ 0.9 V/dec, respectively. After laser annealing with a fluence of 0.43 J/cm²/pulse, those values were changed to 0.6 V, $\sim 3.2 \times 10^4$, 78.6 cm² V⁻¹ s⁻¹, and ~ 0.9 V/dec, respectively. The inset details the hysteresis effect, which can be clearly seen before the laser annealing (black curves), but reduced after the laser annealing (red curves). (d) Voltage transfer curves of the inverter before (black squares) and after (red squares) the laser annealing for the depletion mode load. (e) Voltage transfer curves before (black squares) and after (red squares) the laser annealing for the enhanced mode load.

The operating principle of enhancement mode load transistor is different compared to depletion mode load inverter. Figure 3e shows that output voltage was not completely zero even when the input was driven high. Also the transition from high to low was not as sharp as that of the depletion mode. These were primarily due to the static current through M_3 and M_4 when M_4 was turned on. Unlike the depletion mode, the $V_{gs3} - V_{th3}$ increases when V_{OUT} drops, which increases the static current. At this time, the output voltage was determined by the on resistance (R_{ON}) values of M_3 and M_4 as Ohm's law is applicable. Thus, the ratio of pull-up and pull-down transistor was important in this case. In practice, this ratio can be achieved by adjusting the channel length. In addition, high R_{ON} of M_3 was required to obtain a sharper transfer from high to low state. The starting of transition from high to low is at a small negative voltage, as V_{th} of M_4 exists in the slightly negative area. Therefore, the value of NM_L was around 0.3 V before administering femtosecond laser annealing, which is a compromised operation. The femtosecond laser annealing produced a selective positive shift of V_{th} for M_4 . As a result, the value of NM_L increased to around 1.2 V.

Meanwhile, NM_H decreased from around 0.9 to 0.3 V, due to the positive threshold voltage shift. However, the total noise margin, $NM_L + NM_H$, increased from 1.2 to 1.5 V. Therefore, femtosecond laser annealing improved noise immunity by increasing the total noise margin, $NM_H + NM_L$. Figure 3e shows the effect of femtosecond laser annealing on an enhancement mode inverter: the trip voltage was shifted to the positive direction toward half of the supply voltage, and the total noise margin was improved. The hysteresis of this inverter was more prominent than that of the depletion mode, and we are investigating the causes and ways to mitigate them.

Finally, our inverter is highly transparent. Figure 4 shows the optical transmission spectra through the fully transparent NMOS inverters using In₂O₃ nanowires on a glass substrate in the 350–1250 nm wavelength range. The optical transmission value was $\sim 82\%$. Note that the optical transmission value of corning glass substrate is $\sim 92\%$. The NWT array regions were 1.0×0.5 in. (the glass substrate was 1.5×1.0 in.) and contained ~ 1500 NWT device patterns; and the entire substrate was coated with the Al₂O₃ gate insulator. The source/drain regions and the gate

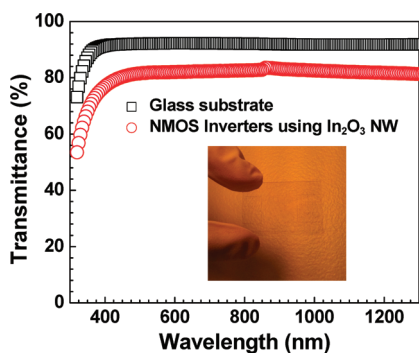


Figure 4. Optical transmission spectrum through the entire NWT inverter structures. The inset shows the high transparency of the substrate with 1500 NWT inverter devices; with the texture on the layer below the substrate clearly visible.

regions covered $\sim 40\%$ and $\sim 60\%$ of the total NWT array region, respectively. Since In_2O_3 nanowires do not cover much of the entire NWT array and the diameter of the NWs was only 20 nm, their optical absorption was negligible. The inset in Figure 4 shows the substrate with fully transparent NMOS inverters over an opaque layer. The texture on the paper is clearly seen through the device substrate.

In conclusion, it is important to improve the performance of as-fabricated nanowire devices as they typically suffer from weak saturation and unpredictable threshold voltages. The thermal budget of annealing is typically limited by the low-temperature requirements of transparent and flexible substrates. Femtosecond lasers could be focused onto and tune individual NWTs. However, they can also damage the NWTs easily. The direct illumination of nanowires was avoided in our annealing process so that damaging of NWTs did not occur. This was evidenced by the preservation and slight improvement of other major performance parameters, such as mobility, on–off current ratio, and sub-threshold slope. The improvement of current saturation, on the other hand, is desirable in most applications. Since our femtosecond laser photons have energy below the band gap of In_2O_3 nanowires, femtosecond

laser annealing is expected to be mainly thermal, possibly forming an improved single-crystalline In_2O_3 nanowire structure. The short pulse duration may result in ITO photophysical bond breaking instead of classical melting,²² consequently forming ITO spikes into the nanowire channel to improve the contact-channel interface, modifying the Schottky barrier height and the effective doping in the nearby semiconductor region. Further investigation of the mechanism behind such annealing effects is interesting and ongoing. This study provides insights into the contact-dominated transistor properties, in terms of the effects on output resistance and V_{th} .

Combined with the excimer laser annealing,¹³ which shifts the threshold voltage to the negative direction by increasing the number of oxygen vacancies, one could envision full trimming capability of the threshold voltages of NWTs and maintaining high current saturation, thus opening the possibility of constructing sophisticated circuit blocks or other functional devices made from NWTs, and significantly advance our knowledge on flexible, and transparent electronics on low-temperature substrates. Controlling the threshold voltages of nanowires is of central importance to any practical integrated circuits. The semiconductor industry enjoys highly uniform doping and high-precision manufacturing (*i.e.*, critical dimension control) to achieve uniform threshold voltages. While manufacturing of non-Si nanowire based transistors will certainly improve with novel techniques, it is unlikely that they will match the level of control in CMOS technologies, therefore the femtosecond laser tuning of individual NWT presented here would be very important in manufacturing NWTs if large circuit blocks are to function as designed. We note that there could be other ways to alter the transistor characteristics, such as surface passivation and chemical modifications. Femtosecond laser annealing appears to be noninvasive, and still preserves the flexibility of applying the above-mentioned tuning process. Thus it would be a useful trimming method for future NWT-based integrated circuit manufacturing.

METHODS

Femtosecond Laser Anneal and I–V Measurement. The laser annealing source was a Ti:Sapphire laser operating at 800 nm. The laser pulse duration was 50 fs and the repetition rate was 1 kHz. Laser transmitted power varied from 1.67 μW (average energy fluence rate of 0.14 $\text{J}/\text{cm}^2/\text{pulse}$) to 5 μW (average energy fluence rate of 0.43 $\text{J}/\text{cm}^2/\text{pulse}$). The transmission spectra of normal incident linearly polarized light were collected with a Lambda 950 spectrophotometer (Perkin-Elmer). Electrical characterizations was performed with a semiconductor parameter analyzer (HP 4156A).

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